voltage is selected to reverse bias said switching diode.

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15. The electronic device of claim 9, wherein said first voltage is selected to reverse bias said switching diode.

REMARKS

Claims 1 through 15 are pending in the present application. Claims 14 and 15 were newly added.

The Office Action dated June 19, 2002, rejected claims 1 through 13 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,728,802 to Baron ("the Baron patent"). Also, claims 6 through 13 were objected to under 37 C.F.R. 1.75(c) as being in improper dependent form.

It is respectfully submitted that present claim 1 defines an invention that is neither disclosed nor suggested by the Baron patent. The Baron patent is directed to an electronic matrix system 10 forming a photosensitive pixel array 11. Each pixel 22 of array 11, as suggested by the Examiner, has an isolation means composed of two blocking diodes 34,36 arranged in series. (col. 6, lines 32-36) In addition, each pixel 22 has a photogenerative element 40 electrically connected to a common node 38 formed by blocking diodes 34,36 and to a common address line 18. (col. 6, lines 54-57) Further, input lines R_1 and R'_1 receive drive signals from a row select driver 50 to apply first operating potentials equal in magnitude and opposite in polarity about node 38 to forward bias or turn on blocking diodes 34,36 and to apply second operating potentials equal in magnitude and opposite in polarity about node 38 to reverse bias or turn off

blocking diodes 34,36. (col. 7, lines 18-35) This balanced node approach overcomes the capacitive kick problem. Since the driving voltages are balanced (i.e. of equal magnitude and opposite polarity) relative to node 38, the transient currents flowing through the blocking diodes 34,36 are also balanced, and these transient currents cancel one another. Thus, there is no current flow into the element 40, so the voltage at node 38 remains at a constant potential immediately after the blocking diodes 34,36 have switched from their conducting to nonconducting state. (col. 10, lines 49-58) The benefit achieved by this arrangement is that the size of the capacitances of the blocking diodes 34,36 relative to the capacitance of element 40 is of less importance to the sensitivity/accuracy of reading element 40.

In contrast, claim 1 defines an invention directed to removing DC offset current and reducing the number of diodes required for multiplexer circuits. It is respectfully submitted that these objectives are achieved via a circuit arrangement that is clearly distinct from that which is disclosed by the Baron patent. The multiplexer circuit of claim 1, for <u>each input line 2</u>, as opposed to the every two input lines (R1, R'1), (R2, R'2), and (R3, R'3) disclosed in the Baron patent, has a diode clamp 5 with first and second clamp terminals 6,7 and first and second clamp diodes 8,9, as well as isolation means, such as an isolation diode 10, provided between each input line 2 and the common output. This circuit/diode arrangement beneficially eliminates offset voltages introduced during the second mode of operation, thereby eliminating the need to remove consequential offset currents added to the signal. Clearly, the input line differentiation technique enabled by the diode-circuit arrangement of claim 1, is beyond that which is

disclosed or suggested by the Baron patent.

Thus, it is respectfully submitted that claim 1 is patentable over the cited reference. Accordingly, reconsideration and withdrawal of the rejection, and allowance of claim 1, are respectfully requested.

It is also respectfully submitted that claims 2 through 5, which depend either directly or indirectly from claim 1, are patentable at least for the reasons stated above with respect to claim 1.

Regarding independent claim 6, it is respectfully submitted that the invention of claim 6 is neither disclosed nor suggested by the Baron patent. Claim 6, similar to claim 1, requires a multiplexer circuit having, for each input line 2, a diode clamp 5 with first and second clamp terminals 6,7 and first and second clamp diodes 8,9 arranged in series with the same polarity between said clamp terminals, and isolation means 10 between each input line and said common output. Thus, claim 6 is patentable, at least for the reasons stated above with respect to claim 1.

Regarding claims 7 through 13, each of these claims depend either directly or indirectly from claim 6, and thus, similar to claim 6, are patentable at least for the reasons stated above with respect to claim 1.

Regarding claims 14 and 15, it is respectfully submitted that these claims have been added and fail to disclose any new subject matter. Further, as claims 14 and 15 depend indirectly from claim 6, similar to claim 6, the claims are patentable at

least for the reasons stated above with respect to claim 1.

In sum, it is respectfully submitted that the pending claims are clearly patentable over each cited reference. Thus, this application is in condition for allowance. Accordingly, reconsideration and withdrawal of all rejections of the claims are respectfully requested.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend claims 1 through 13 and add claims 14 and 15 as follows:

1. (Amended) A multiplexer circuit for switching a selected one of a plurality of current inputs carried by respective input lines to a common output, [the] said circuit comprising, for each input line:

a diode clamp comprising first and second clamp terminals and first and second clamp diodes arranged in series with the same polarity between [the] said clamp terminals; and

isolation means provided between each input line and [the] said common [terminal] output,

wherein [the] said diode clamp is operable in two modes, a first mode in which voltages are applied to [the] said clamp terminals such that [the] said diodes of [the] said diode clamp are forward biased and hold [the] said input line at a first voltage which prevents [the] a passage of current from [the] said input line to [the] said common output, and a second mode in which the voltages are applied to [the] said clamp terminals such that [the] said diodes of [the] said diode clamp are reverse biased and [the] said passage of [the] said current from [the] said input line to [the] said common output is allowed.

2. (Amended) [A] The multiplexer circuit [as claimed in] of claim 1, wherein [the] said isolation means [comprises] has

an isolation diode.

3. (Amended) [A] The multiplexer circuit [as claimed in] of claim 2, wherein [the] said first voltage is selected to reverse bias [the] said isolation diode, thereby preventing [the] said passage of current from [the] said respective input line to [the] said common output.

4. (Amended) [A] The multiplexer circuit [as claimed in] of claim 1, wherein [the] said isolation means [comprises] has a capacitor.

5. (Amended) [A] The multiplexer circuit [as claimed in] of claim 4, wherein [the] said first voltage is selected depending on [the] a source of [the] an input current, such as to prevent current flowing from [the] said source of [the] said input current.

6. (Amended) An electric device comprising:

an array of charge storage elements [which] that are arranged in rows and columns and which are coupled to row and column conductors, [the] said column conductors being arranged in at least one group, each group having a respective common output[,];

a multiplexer circuit [as claimed in claim 1] for switching a selected one of a plurality of current inputs carried by respective input lines to said common output, said multiplexer circuit having, for each input line, a diode clamp with first and second clamp terminals and first and second clamp diodes arranged in series with the same polarity between said

clamp terminals; and isolation means between each input line and said common output, wherein said diode clamp operates in a first mode in which voltages are applied to the clamp terminals such that said diodes of said diode clamp are forward biased and hold a first voltage that prevents the passage of current from said input line to said common output, and a second mode in which said diodes of said diode clamp are reverse biased allowing for the passage of a current from said input line to said common output, said multiplexer circuit [coupling the] couples said column conductors of [the] said respective groups to [the] said respective common output[,]; and

a charge measurement device [which] that measures [the] a flow of charge from [the] said common output.

7. (Amended) [An] The electronic device [as claimed in] of claim 6, wherein [the] said charge storage elements [comprise] have photosensitive pixels including a photodiode and a switching diode.

8. (Amended) [An] The electronic device [as claimed in] of claim 7, wherein [the] said isolation means [comprises] has an isolation capacitor.

9. (Amended) [An] The electronic device [as claimed in] of claim 8, wherein during [the] said second mode charge flows from each input to [the] said respective isolation capacitor, and wherein [the] said diode clamp is operable in a third mode in which voltages are applied to [the] said clamp terminals such that [the] said diodes in [the] said diode clamp are forward biased and hold [the] said input line at a second voltage which causes charge stored on the isolating capacitor to flow between

the isolation capacitor and the charge measurement device.

10. (Amended) [An] The electronic device [as claimed in any one of claims 7 to 9] of claim 7, wherein [the] said first voltage is selected to reverse bias [the] said switching diode.

11. (Amended) [An] The electronic device [as claimed in] of claim 6, wherein [the] said charge storage elements comprise capacitive pixels [including] having two diodes and a variable capacitor, the current measurement being used to determine the capacitance.

12. (Amended) [An] The electronic device [as claimed in] of claim 11, wherein [the] said isolation means [comprises] has an isolation diode.

13. (Amended) [An] The electronic device [according to] of [Claim] claim 11, wherein [the] said pixels [comprise] have capacitive fingerprint sensing elements in which the capacitance of [the] said variable capacitor is determined by a fingerprint portion overlying [the] a pixel.

NEWLY ADDED CLAIMS:

14. The electronic device of claim 8, wherein said first voltage is selected to reverse bias said switching diode.

15. The electronic device of claim 9, wherein said first voltage is selected to reverse bias said switching diode.